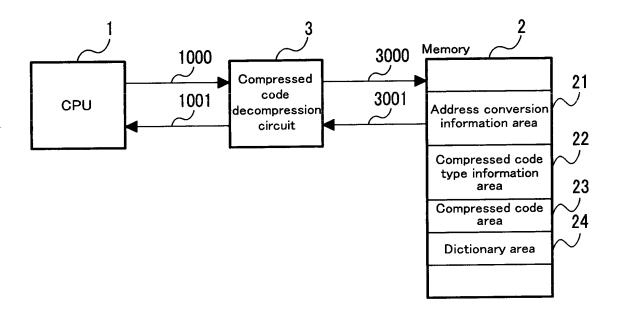
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FIG.1

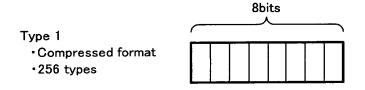


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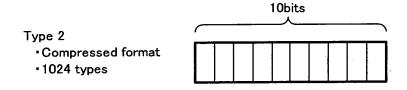
# FIG.2A



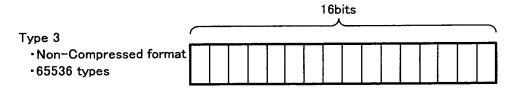
# FIG.2B



# FIG.2C



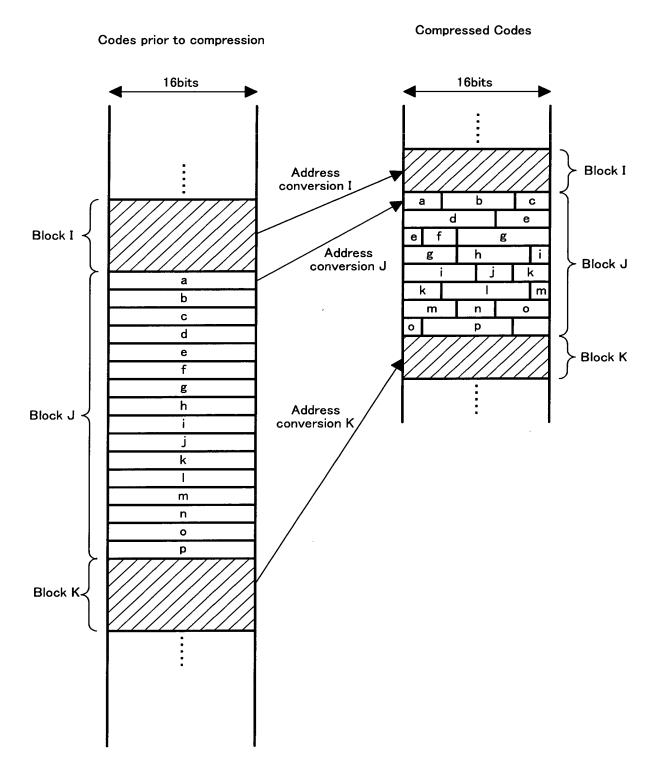
# FIG.2D



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### FIG.3A

# FIG.3B



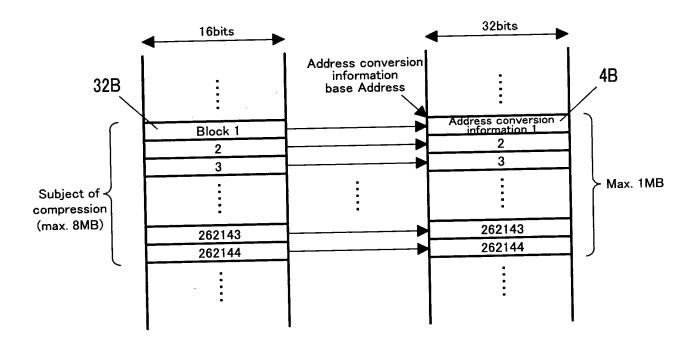
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FIG.4A

FIG.4B

Codes prior to compression

Address conversion information



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FIG.5

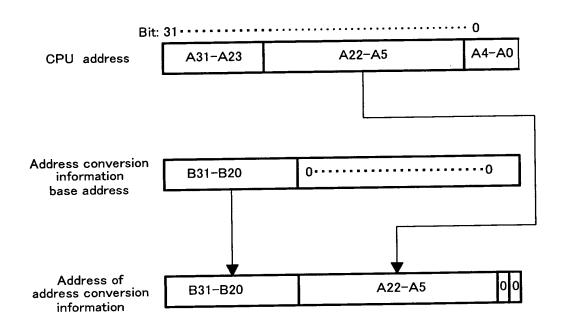
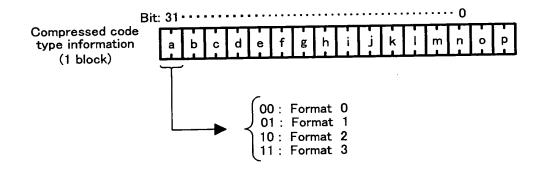
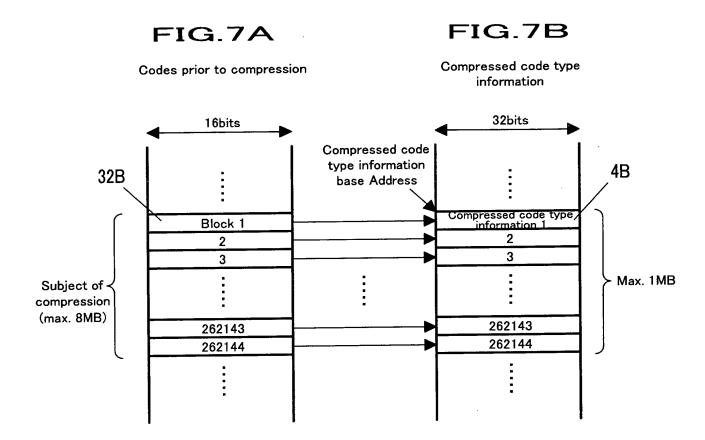


FIG.6

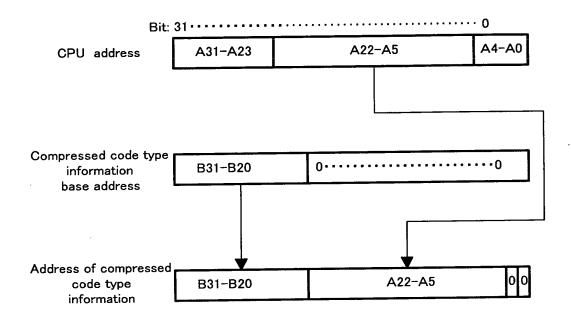


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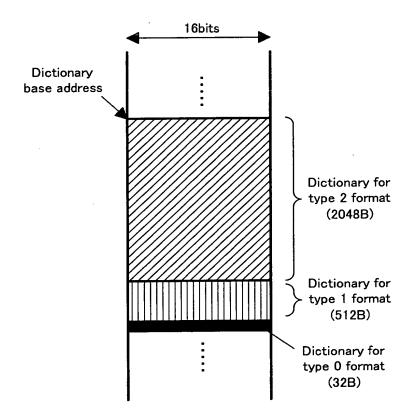
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FIG.8



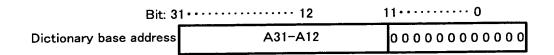
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FIG.9

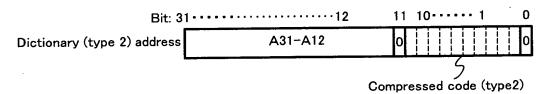


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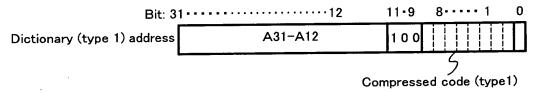
#### FIG.10A



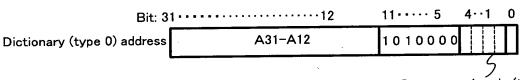
# **FIG.10B**



### **FIG.10C**



### **FIG.10D**



Compressed code (type0)

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FIG.11

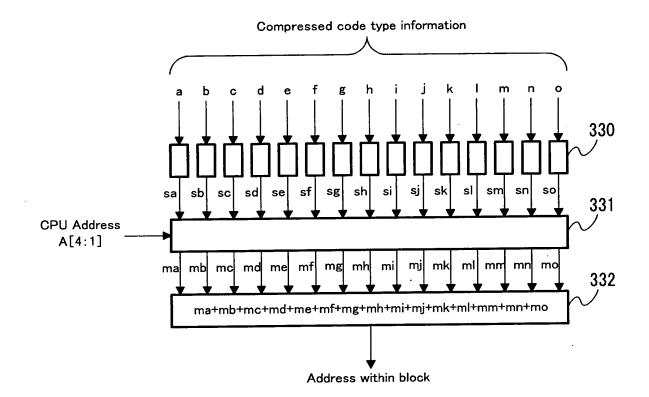


FIG.12

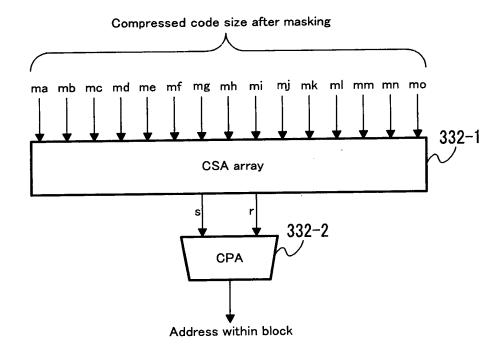
Input i	Output o				
00	0010				
01	0100				
10	0101				
11	1000				

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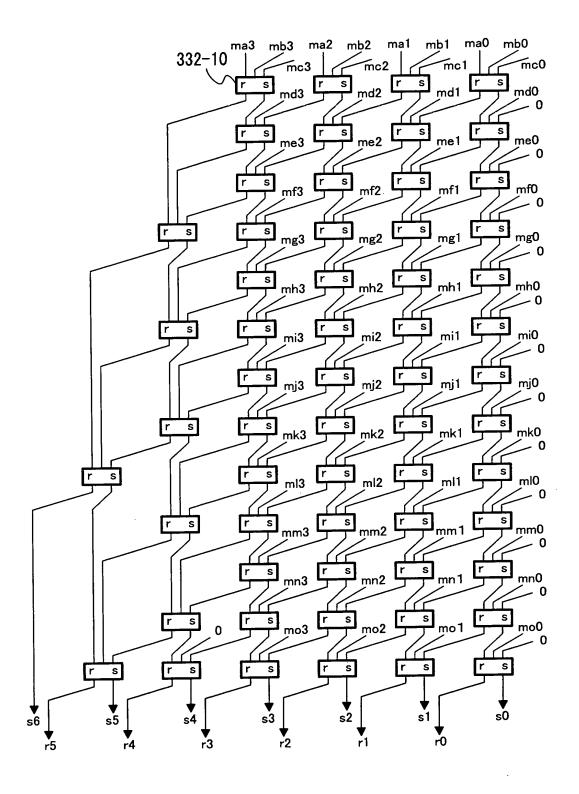
A[4:1]	ma	mb	mc	md	me <sup>·</sup>	mf	mg	mh	mi	mj	mk	ml	mm	mn	mo
0000	z	z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0001	sa	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0010	sa	sb	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0011	sa	sb	sc	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0100	sa	sb	sc	sd	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0101	sa	sb	sc	ba	se	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0110	sa	sb	sc	sd	se	sf	Z	Z	Z	Z	Z	Z	Z	Z	Z
0111	sa	sb	sc	sd	se	sf	sg	Z	Z	Z	Z	z	Z	Z	Z
1000	sa	sb	sc	sd	se	sf	sg	sh	Z	Z	Z	Z	Z	Z	Z
1001	sa	sb	sc	sd	se	sf	sg	sh	si	Z	Z	Z	Z	Z	Z
1010	sa	sb	sc	sd	se	sf	sg	sh	si	sj	Z	Z	Z	Z	Z
1011	sa	sb	sc	sd	se	sf	sg	sh	si	sj	sk	z	Z	Z	Z
1100	sa	sb	sc	sd	se	sf	sg	sh	si	sj	sk	sl	Z	Z	Z
1101	sa	sb	sc	sd	se	sf	sg	sh	si	sj	sk	sl	sm	Z	Z
1110	sa	sb	sc	ba	se	sf	sg	sh	si	sj	sk	sl	sm	sn	Z
1111	sa	sb	sc	sd	se	sf	sg	sh	si	sj	sk	sl	sm	sn	so

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FIG.14



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FIG.16

iO	i1	i2	r	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

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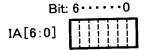
# FIG.17A

Address conversion information (head address of compressed code block)



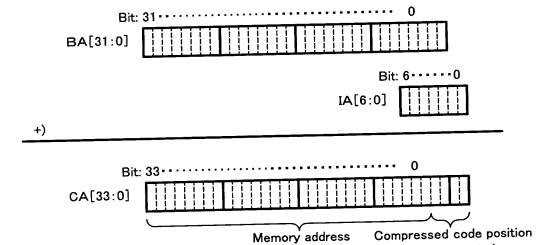
### **FIG.17B**

Address within block



# FIG.17C

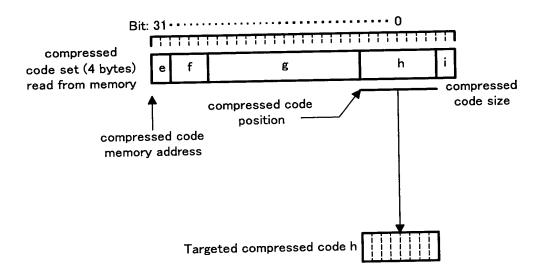
Compressed code Address



(in 4-byte units)

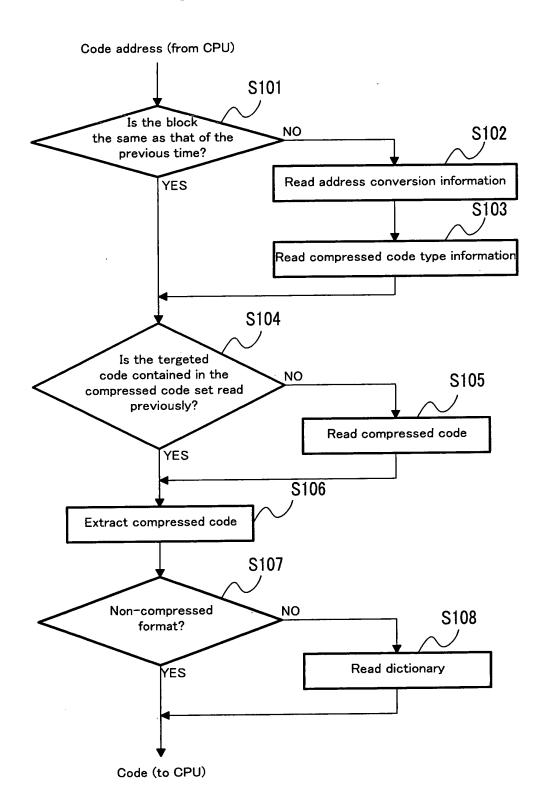
(in 2-bit units)

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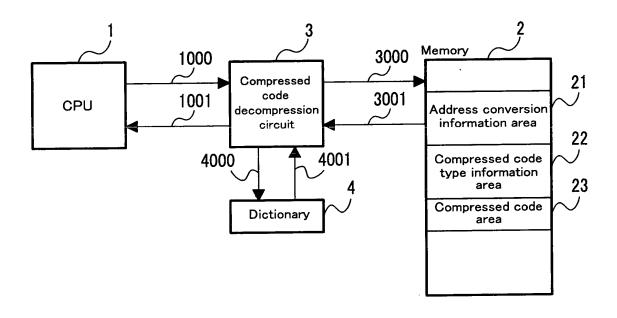


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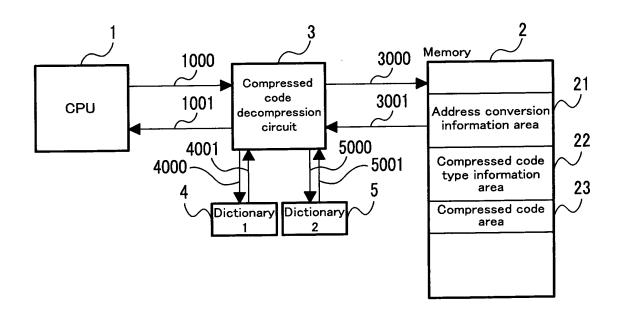
FIG.19



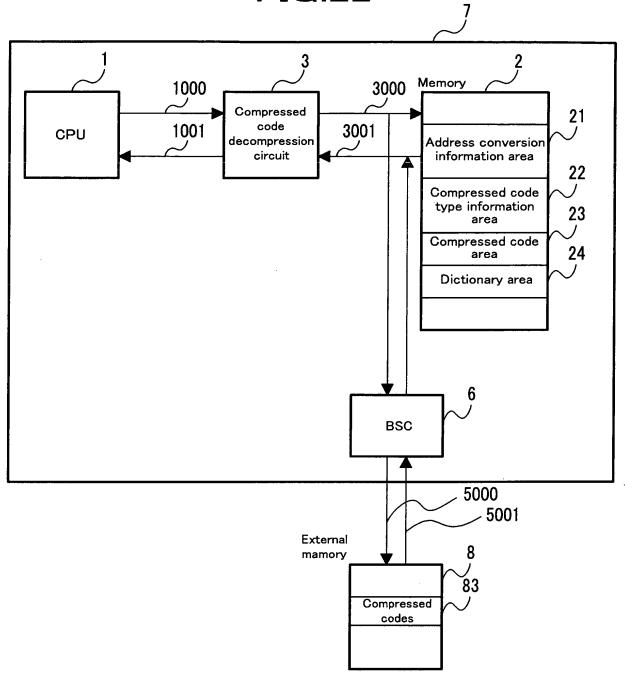
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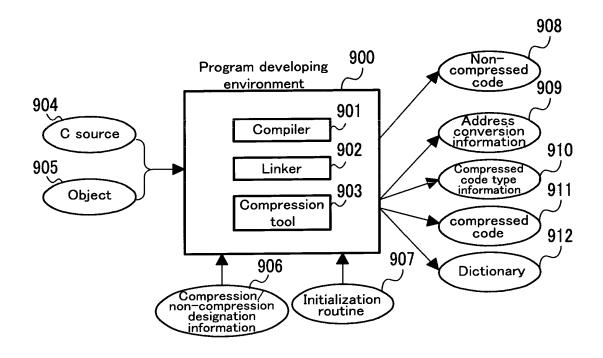
**FIG.21** 



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**FIG.24** 

